Texture and Microstructure Investigation of Cu Damascene Interconnects

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Introduction

As the features of integrated circuitry (IC) chips are scaled down to submicron dimensions, the manufacturer demands new technology to meet performance and reliability requirements for the electronic interconnects. According to these technical demands, the copper damascene process became an important issue in the integrated circuitry (IC) chips industry since it allows a decrease in RC (resistance and capacitance) delay losses, reduces the number of processing operations and increases the lifetime of the interconnect lines. Since the Cu damascene process has been introduced in the IC chips industry, significant research on the relationship between texture and reliability of copper interconnects has been undertaken. It is well known that strong {111} texture increases the resistance of electromigration failure and this failure can be correlated with the frequency of the occurrence of CSL (coincidence site lattice) boundaries or low or high diffusivity boundaries and the strength of {111} texture in aluminum thin films. However, such a relationship for the Cu hasn't been firmly established and the driving forces which can affect the textural evolution during annealing were not clearly identified until now. In this study, the details of textural and microstructural evolution during annealing will be examined using orientation imaging microscopy (OIM).

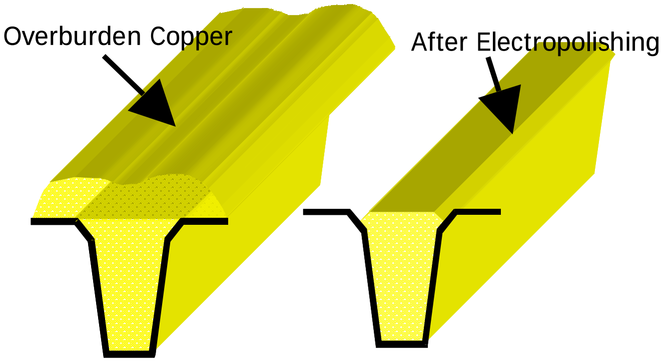


Figure 1 – Schematic of sample preparation for Cu damascene interconnects

OIM Measurements

Two different samples, one as-deposited and another annealed were used for this investigation. Both samples were fabricated using the same conditions and were kept at room temperature for 6 months. TaN, 400Å thick, was deposited on the surface of the Si (100) wafer as the barrier layer, and then a copper seedlayer was deposited on the barrier layer. The trenches were filled with copper by electroplating in a sulfuric acid bath using 24 mA/cm^2 current density. Then, the samples were annealed at 200°C for 10 minutes in the vacuum furnace to avoid oxide formation on top of Cu interconnects. Each sample has different line widths from 0.14 to 2 μm and every line has the same trench depth of 0.7 μm. To remove the overburden of Cu damascene interconnects, the samples were electro-polished for 120 seconds in a H_3PO_4 solution using 17 mA/cm^2 current density (figure 1). After electropolishing, the top surface area of the trench was analyzed using the orientation imaging microscope (OIM) mounted on a Philips XL30 FEG-SEM to identify the orientation of each grain and type of grain boundaries in the copper interconnects. Misorientation between grains was measured and classified as CSL (The coincidence site lattice) and non-CSL boundaries. The frequency of occurrence of CSL boundaries up to $\sum$29 was calculated.

Texture of Cu damascene interconnects

To obtain quantitative information about texture, three pole figures were measured from the top surface of Cu interconnects using OIM. The results presented in figure 2, indicate that {111}<110> textures exist in all samples, however it becomes fiber-like textures as the line width increases. Compared to the “as-deposited” sample, the texture of the **“**annealed” sample becomes stronger. The maximum intensity is the strongest in the narrowest line and it decreases as the line width increases. The difference between the “as-deposited” and “annealed” sample in intensity is highest for the narrow lines and it decreases as the line width increases. In addition, a weak {111} sidewall component was found in the narrow lines, such as 0.14, 0.24 and 0.5 μm line width, as shown in figure 2. The strength of the sidewall {111} component changes as the line width increases: the strongest intensity was found at the narrowest lines, and it decreases when the line width increases up to 1 μm, and then increases to 2 μm line width in both specimens. The intensities of the “annealed” sample are always higher than the “as-deposited” sample. It seems that the annealing process minimizes the sidewall contribution to overall texture in the Cu interconnects.

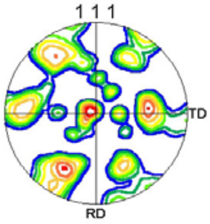
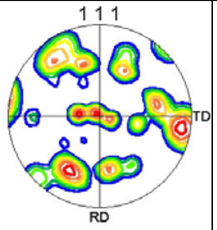
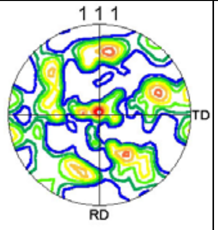
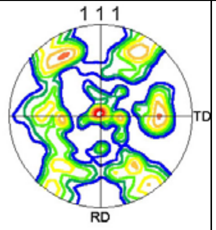
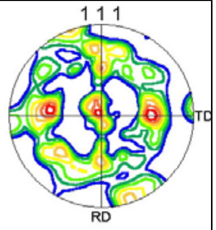
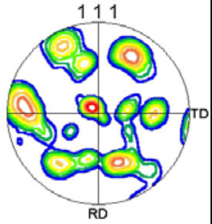
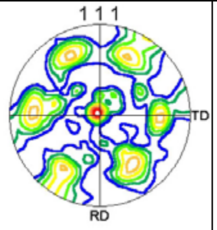
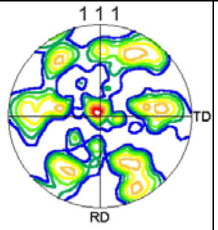
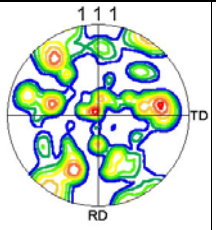
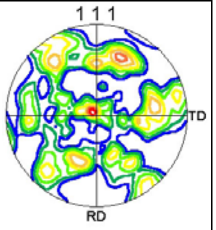
Line Width	**0.14 μm**	**0.24 μm**	**0.5 μm**	**1 μm**	**2 μm**
As-deposited	 Max = 8.697	 Max = 6.577	 Max = 5.512	 Max = 5.648	 Max = 3.915
Annealed	 Max = 14.054	 Max = 8.878	 Max = 6.043	 Max = 6.094	 Max = 4.056

Figure 2. {111} Pole figures of copper interconnects having a different line width: as-deposited samples and after 200°C annealing.

Microstructure of Cu damascene interconnects

To analyze microstructural evolution after electropolishing, the orientation of grains and types of grain boundaries on the top area of the Cu interconnect were measured by the EBSD technique, as shown in figure 3. These inverse pole figure maps demonstrate that the so-called bamboo structure is found in 0.14 μm line and semi-bamboo structure is observed in 0.24 and 0.5 μm line width samples. However, 1 and 2 μm lines show a polycrystalline microstructure with a mixture of large and small grains. Regardless of the difference in line width, all Cu interconnects investigated show a high number of twin boundaries. After annealing, it seems that the microstructure of Cu interconnects contain less twin boundaries and grains are larger.

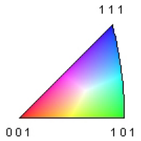
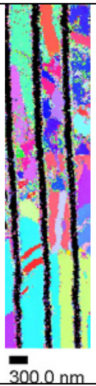
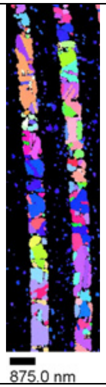
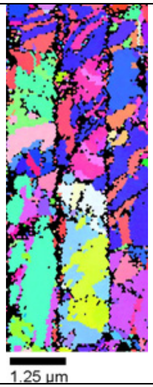
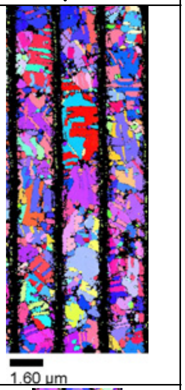
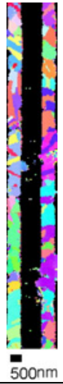
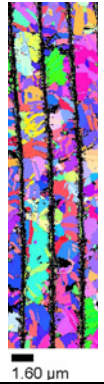
Line Width	0.14μm	0.24μm	0.5μm	1μm	2μm
As-deposited 					
Annealed					

Figure 3. Inverse pole colored map representing orientation of planes parallel to the surface of the interconnect lines after electropolishing.

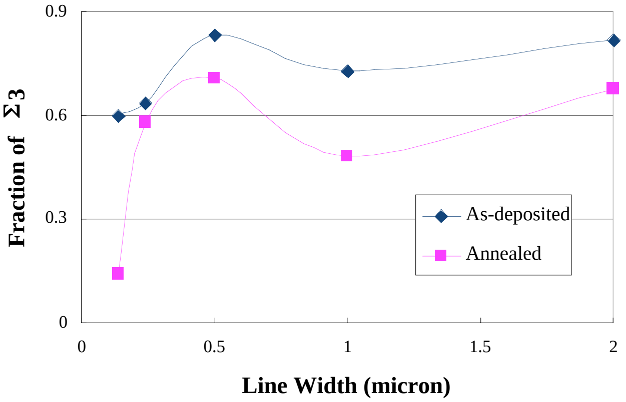


Figure 4. Σ3 CSL boundaries in Cu interconnects lines having a different line width after annealing

The frequency of CSL (coincidence site lattice) boundaries as measured by the EBSD technique is shown in figure 4. The results obtained demonstrate that the fraction of Σ3 boundaries increases as the line width increases. Also, a higher fraction of twin boundaries is observed in the 2 μm line. However, after annealing, this fraction decreases, especially in the 0.14 μm line width interconnects sample. From these results, it can be concluded that the annealing process enhanced the grain growth of Cu interconnects consuming the twin boundaries.

Summary

Textural and microstructural evolution of Cu interconnects after annealing was found: the {111} <110> texture component increases and the {111} sidewall components decreases. However, the effect of the sidewall component on the overall texture of Cu interconnects is negligible if annealing affects the textural and microstructural evolution during annealing. The fraction of the Σ3 boundaries increases as the line width increases, however it decreases after annealing because the grain growth is dominating in the Cu interconnects.

Bibliography

For more details on this work see the following papers:

1. "Textural and Microstructural Transformation of Cu Damascene Interconnects after Annealing " by **J.Y. Cho**, H.J. Lee, H. Kim and J.A. Szpunar, Journal of Electronic Materials, Vol. 34, No 5, pp. 506-514 (2005)
2. "Texture Investigation of Copper Interconnects with a Different Line Width" by **J.Y. Cho**, K. Mirpuri, D.N. Lee, J.-K. An and J.A. Szpunar, Journal of Electronic Materials, Vol. 34, No 1, pp. 53-61 (2005)
3. "Textural Evolution of Cu Damascene Interconnects after Annealing" by **J.Y. Cho**, H.J. Lee, H. Kim and J.A. Szpunar, 2004 MRS Spring Meeting Proceeding, Symposium F on *Materials, Technology, and Reliability for Advanced Interconnects and Low-k Dielectrics*, Vol. 812, F8.9 (San Francisco, CA, USA)